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UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD., a Taiwan Corporation, Plaintiff, v. TELA INNOVATIONS, INC., a Delaware Corporation, Defendant.	Case No. 5:14-cv-362 **COMPLAINT FOR FRAUD; BREACH OF CONTRACT; TRADE SECRET MISAPPROPRIATION** **DEMAND FOR JURY TRIAL** Date Filed: Trial Date:

Plaintiff Taiwan Semiconductor Manufacturing Company, Ltd. ("TSMC") alleges as follows:

NATURE OF THE ACTION

1. Defendant Tela Innovations, Inc. ("Tela") fraudulently induced TSMC to disclose TSMC's confidential Design Rules with an intention to use information about those rules to shape the claims of its patent applications to claim subject matter that Tela did not invent, but that Tela believed (incorrectly, as it turns out) would read onto products designed in accordance with TSMC's Design Rules. Tela also has breached several non-disclosure agreement(s) with TSMC by disclosing to its patent agents and misusing confidential and trade secret information about TSMC's design rules, process requirements, and engineering analysis to shape the claims of Tela's patent applications to claim subject matter that Tela did not invent, but that Tela believed would read onto products designed in accordance with TSMC's Design Rules. On information and belief, Tela also has breached and is continuing to breach the terms of a collaboration agreement by offering and/or licensing cell libraries and layouts that Tela created by practicing the inventions claimed in Tela patents while those patents were licensed for exclusive use by TSMC. TSMC seeks damages and injunctive relief.

PARTIES

2. Plaintiff TSMC Ltd. is a Taiwanese corporation organized in 1987 that maintains its principal place of business at No. 8 Li-Hsin Road 6, Hsinchu Science Park, Hsinchu, Taiwan 30077. TSMC is recognized worldwide as the world's most advanced and most successful provider of semiconductor fabrication services for customers who design their own circuit layouts, but who either lack their own semiconductor manufacturing expertise and facilities, or simply wish to use TSMC's high quality fabrication services or technology. TSMC owns and operates twelve "fabs" in Taiwan.

3. Tela is a Delaware corporation organized in June, 2005 that maintains its principal place of business at 485 Alberto Way, Suite 115, Los Gatos, California 95032.

JURISDICTION AND VENUE

4. This Court has jurisdiction over this action pursuant to 28 U.S.C. § 1332(a)(2), because Plaintiff is a corporation organized and existing under the laws of Taiwan having its principal place of business at No. 8 Li-Hsin Road 6, Hsinchu Science Park, Hsinchu, Taiwan 30077, and Defendant is a corporation incorporated under the laws of the State of Delaware, and having its principal place of business in the State of California. The amount in controversy exceeds $75,000, exclusive of interest and costs.

5. Venue is proper in this District under 28 U.S.C. § 1391(b)(1), as this is the District in which Tela resides. Furthermore, pursuant to Civil L.R. 3-2, assignment of this action to the San Jose Division of this Court is proper because a substantial part of the events or omissions that give rise to TSMC's claims occurred in Santa Clara County, where, on information and belief, Tela is headquartered.

FACTUAL ALLEGATIONS

A. Semiconductor Wafer Fabrication

6. Integrated circuits (also known as "chips" or "ICs") are the small electronic devices present in all modern electronic products. They contain millions of microscopic electrical components (*e.g.*, transistors, resistors, etc.), each with a dimension less than a micron ("µm") in size. These components are embedded in the silicon substrate of a wafer. The components within each chip are interconnected with stacked layers of ultra-fine metallic traces (wires), after which the wafer is divided into hundreds or even thousands of die, which are then cut, assembled, and sold as integrated circuits to electronic product manufacturers. Many of the world's leading designers of integrated circuits—including just about every major California high-technology company—use TSMC to fabricate wafers from their chip designs.

7. Transistors are the heart of integrated circuits and are formed within a silicon substrate, called a wafer. A transistor is a switch that can turn on and off billions of times per second. It consists of "source" and "drain" regions, which are separated from one another by a "gate." The gate, which is made from a material such as polysilicon, controls the flow of

electricity from the source to the drain, and thus whether the transistor is "on" or "off." Even when the gate is closed and the transistor is off, however, some amount of electrical current may flow from the source to the drain, giving rise to leakage and undesired power consumption. It has been known for decades that both the amount of leakage, and the on/off speed of the transistor, can be controlled by adjusting or "biasing" the length of the polysilicon gate.

8. One or more layers of thin metal lines that run above the substrate and the gate layer are used to connect transistors and other components to one another, to carry power to the transistors, and to link the circuitry to external connections at the edge of the chip. For many generations, chips have contained multiple metal interconnect layers stacked above one another, with the first layer above the substrate called Metal 1 or "M1" and the next layer up called Metal 2 or M2, etc. A complex chip design may require as many as ten layers of metal.

9. As semiconductor process technology has advanced over the years, manufacturers have been able to fit more electrical components onto the same size piece of silicon. Thus, any given semiconductor manufacturing process has an associated "process technology node," which is identified by the size of the smallest dimension of a feature made using the process, such as the width of a transistor gate, or the width of a metallic interconnect wire. The more advanced process technology nodes in use today, depending on the sophistication of the manufacturer, are 65 nanometer ("nm"), 45 nm, and 28, 22 and 20 nm (1 micron (µm) equals 1000 nanometers). A typical human hair is 50 to 100 µm in diameter—5,000 times thicker than the smallest feature on a 20 nm chip.

10. Each year, TSMC invests hundreds of millions of dollars in research and development to stay on the cutting edge of integrated-circuit fabrication by making circuit features smaller and more efficient with each new generation of technology. The smaller the overall area of the IC (called a "die," of which there may be hundreds on a single wafer), the lower its cost. The industry expects that an advanced manufacturer like TSMC will be able to introduce a new and smaller process node approximately every two years targeted to obtain around a 50% reduction in chip area, but with comparable or better performance.

11. Beginning at the .18 µm node (180 nm), the size of the smallest feature became less than the 193 nm wavelength of the light used to create it, requiring optical corrections in the mask patterns simply to create a square corner. As process nodes have continued to decrease in size below 90 nm, the physics of light transmission, and electron flows, and material science have posed ever more challenging processing conditions, which in turn have necessitated more stringent design rule restrictions and narrowed design flexibility. TSMC's R&D operation employs thousands of engineers dedicated to perfecting each new generation of process node and to overcoming the challenges associated with ever decreasing size.

12. TSMC has developed a proprietary information-protection policy that secures IP confidentiality company-wide. TSMC deploys several measures, both electronic and physical, to protect its IP, including marking its documents with various levels of security, restricting access to documents and to the fabs themselves to persons who have a need to know, and entering into non-disclosure agreements with customers and third parties with whom TSMC must collaborate to operate its business.

B. The Chip Design Process

13. For TSMC to fabricate a wafer, its customers provide an integrated-circuit design (comparable to a blueprint) that describes the components desired by the customer and the way they will be interconnected. TSMC will then take the data it receives about the circuit design layout from the customer and use it to create patterned "masks" through which light will be directed to form the patterns of the chip circuitry, which is called photolithography. At a high level of abstraction, the circuitry is fabricated by bombarding the silicon substrate with electrical particles to form electrically active and non-active regions and then sequentially exposing various layers formed on the silicon to photolithographic exposures through different masks, with dozens of intervening processing steps between each photolithographic exposure.

14. In order for a customer's design to be fabricated using TSMC's manufacturing processes, the design must comply with certain "Design Rules" that TSMC develops for each of its process technology nodes and for each of the general types of chips that can be made at a

given node, for example, a low power processor made using 65 nm technology. Design rules provide the customer with parameters for the type, size and shape of the features and the spatial relationships between features that the customer can use to create its circuit designs. For example, if the process cannot reliably insulate two wires if they are spaced less than 0.2 µm (two ten millionths of a meter) apart, the design rule would specify a minimum separation between wires of 0.2 µm. TSMC develops its design rules through a lengthy, intensive process that involves considerable investments of time and money. Because design rules are an important and competitively sensitive aspect of TSMC's technology, TSMC treats its Design Rules and Design Rule Manuals as highly confidential, proprietary information. TSMC requires its customers, and others to whom TSMC might need to disclose its Design Rules, to execute non-disclosure agreements before TSMC will make them available.

15. Using TSMC's Design Rules and Design Rule Manuals for each new process node, some of TSMC's customers, especially TSMC's larger customers, create their own cell libraries, each containing dozens or hundreds of TSMC Design Rule compliant cells that contain a blueprint for a repeatable unit of transistors, polysilicon lines, interconnect structures, and other features that can be selected and configured together to perform a particular function within a chip. There may be different libraries at the same process node for different kinds of chips, and different cells within a library to perform a common function, each having a different advantage. For instance, a customer wishing to minimize power consumption in a chip that will be battery powered may choose a particular cell library designed for energy efficiency, while a customer hoping to increase speed and performance may choose differently. Each cell is akin to the blueprint for a type of room, including its furniture, fixtures, and wiring, that can later be fabricated as part of a building. The transistors within a cell can be linked together in multiple ways using polysilicon lines insulated from the substrate and/or the wires in the thin metal interconnect wires in the Metal 1 or higher metal layers above the gate layer.

16. Some of TSMC's customers may not have the capability or resources or desire to create their own suite of cell libraries for each new TSMC process technology and type of chip they may seek to have made. TSMC, therefore, has developed its own "standard" cell libraries

that comply with its Design Rules, for use by its customers to design chips for fabrication by TSMC. Third party library vendors like ARM and Synopsis also offer chip designers multiple, standard cell libraries that are TSMC process compliant.

C. In 2006 Tela approached TSMC to help Tela develop a workable, gridded gate-array chip architecture

17. In 2006, Tela approached TSMC claiming to have conceived of a highly regularized circuit architecture for use with process nodes of 90 nm or smaller that Tela believed would save on chip design time and chip area, while boosting performance and the yield of useable "die" on a wafer. Tela described its proposed design solution as employing a "gridded layout," consisting of regularly placed, polysilicon lines available for use as gates and interconnects that would extend in only one common direction across the silicon substrate, with no angled bends or right angled jogs allowed (also called one-dimensional or 1D poly). Tela's design architecture employed a similar grid of regularly placed, 1D metal lines forming the Metal 1 layer, each running perpendicular to the 1D polysilicon lines beneath, followed by another 1D array of lines forming the Metal 2 layer running perpendicular to the Metal 1 layer, and so forth, with each additional metal layer running perpendicular to the layer beneath and above. Tela CEO Scott Becker described this gridded array approach in Provisional Application No. 60/781,288 filed with the United States Patent and Trademark Office ("USPTO") on March 9, 2006. Theoretically, a chip designer could use this gridded architecture to create a circuit layout by placing the source and drain regions of the transistors where desired underneath the array of poly lines, severing the poly lines to create gates, and severing the poly lines and metal lines to create interconnects.

18. As of May 2006, Tela's gridded array design approach was conceptual and only in the earliest stages of testing. Tela did not know if its design approach was useful, or if TSMC's Design Rules could be "pushed" sufficiently to develop a cell library incorporating Tela's approach, or if it would be feasible or cost effective to fabricate a viable integrated circuit from a layout designed using its gridded array approach, or whether the shortened design cycle-time and

circuit performance advantages that Tela touted could actually be realized in practice, and if so, whether they would be outweighed by other disadvantages.

19. Tela wanted to tap into TSMC's process expertise to evaluate the feasibility of Tela's approach, and if feasible, to help co-develop the design of a viable gridded architecture using new design rules and component structures. Tela also asked TSMC to disclose its 65 and 45 nm Design Rules to Tela to permit Tela to propose potential Design Rule changes that might be needed to accommodate its gridded design, which TSMC could then evaluate for manufacturing feasibility and compatibility.

20. On May 16, 2006, TSMC and Tela entered into a Nondisclosure Agreement ("NDA") to begin a collaboration. The Nondisclosure Agreement pertained only to geometries greater than 32 nm. Among other things, that agreement permitted Tela "*only* [to] use [TSMC's] Confidential Information for the purpose of mutually beneficial technical and business developments," and explicitly prohibited Tela "from using such Confidential Information for *any other purposes*." (emphasis added). The Nondisclosure Agreement renews annually unless terminated by prior written notice, and it remains in effect today. Tela further agreed that TSMC would be "entitled to seek proper injunctive or equitable relief in any court of competent jurisdiction in addition to any other remedies by operation of laws or in equity."

21. From May 2006 to January 2009, the parties collaborated to test the viability of Tela's gridded design approach. To enable the collaboration, on July 3, 2006, TSMC mailed Tela a copy of its confidential 65 nm Design Rule Manual, and on December 14, 2007, TSMC provided Tela a copy of its confidential 45 nm design rules. TSMC disclosed to Tela during this time period that certain aspects of Tela's gridded design approach were unnecessary, counterproductive, and not commercially viable. TSMC engineers nevertheless worked with Tela in an effort to create a different cell layout that TSMC's customers might want to purchase and that TSMC would support during fabrication. Through the disclosure of its confidential Design Rules, cell libraries and related information, and in technical discussions and presentations, TSMC also disclosed to Tela the ways in which TSMC's own IC design parameters and approach differed from the invention that Tela had disclosed in its provisional patent application No.

60/781,288 filed with the USPTO on March 9, 2006 - an approach that TSMC told Tela would be a "better option."

22. On November 4, 2008, Tela received US Patent No. 7,446,352 for a "Dynamic Array Architecture," the first patent to mature from its March 9, 2006 provisional application. The '352 patent claims reflected the gridded design elements set forth in that provisional application and that Tela presented to TSMC when it proposed a collaboration in May 2006.

23. Unbeknownst to TSMC, however, on September 17, 2008, just two months before it received the '352 patent, Tela had applied for another patent that claimed subject matter that it did not invent. Tela's Application No. 12/212,562 instead made use of confidential information about TSMC's different and better option for a 45 nm design architecture that TSMC had provided to Tela for their mutual benefit, not for Tela to use for a patent application. Then on March 11, 2009, Tela filed yet another Application No. 12/402,465 for a design that it did not invent, but that similarly made use of confidential information about TSMC's different and better option for a 45 nm design architecture that TSMC had provided to Tela for their mutual benefit, not for Tela to use for a patent application.

D. Tela's fraud, breach of its Non-Disclosure Agreements, and misuse of TSMC's confidential information and trade secret information

24. On January 23, 2009, TSMC and Tela entered into an Area Trim Design Collaboration Agreement, under which they agreed to co-develop 65 and 45 nm cell libraries, layouts and other materials incorporating Tela's and TSMC's technology, though not using the gridded architecture disclosed in Tela's provisional application and the '352 patent.

25. Tela knew that TSMC's 65 nm and 45 nm design rules and cell libraries on which the Area Trim collaboration would focus did not practice at least two essential elements of Tela's gridded design rule invention as claimed in Tela's '352 Patent. But it did not know what TSMC planned for TSMC's newest, 32 or 28 nm process node. Tela intended, but did not disclose to TSMC, its intention to disclose TSMC's information to its patent agents and have them draft and amend the claims of continuation patent applications to attempt to cover products designed in accordance with TSMC's 32/28 nm Design Rules.

26. On March 9, 2009, Tela pressed for TSMC's 32/28 nm rules and an amendment to the parties Nondisclosure agreement to cover them, stating "we need the rules now." In response, TSMC provided, and Tela signed that same day an amendment to the parties' Non-Disclosure Agreement whereby Tela agreed to keep confidential and protect from unauthorized disclosure or use TSMC's 32 nm and smaller technology, and by incorporation of the earlier NDA "*only* to use [such] Confidential Information for the purpose of mutually beneficial technical and business developments." Tela's duty of confidentiality for the 32/28 nm TSMC information disclosed pursuant to the amendment was to be perpetual.

27. Four days later, on March 13, 2009, TSMC provided its 28 nm process Design Rules to Tela. Tela learned from these rules that customers designing products according to TSMC's 28 nm Design Rules would utilize a design approach that differed from, and that would not utilize, an essential element of Tela's patented, gridded array approach.

28. Thereafter, Tela began amending its continuation applications relating to its 1D design approach so as to claim subject matter that it did not invent, but that was designed to attempt to cover products designed in accordance with TSMC's 28 nm Design Rules. Tela did this repeatedly throughout 2009 - 2012.

29. Tela's misuse of TSMC's confidential information is reflected in the claims of at least the following U.S. Patents, Nos. 8,258,547; 8,258,550; 8,258,552; and 8,264,049 (the "Area Trim Patents").

30. In furtherance of its fraud, Tela also misappropriated certain TSMC trade secret information disclosed to Tela in TSMC's 28 nm Design Rules. Tela disclosed the information to its patent agents for incorporation into Tela's Patent Application No. 12/717,887, and used the information to add a limitation to each of the independent claims of that application so as to overcome a rejection by the examiner. Tela's misappropriation of TSMC's trade secret information is reflected in, and allowed Tela to gain allowance of, U.S. Patent No. 8,490,043 (the "'043 Patent").

31. Tela also has disclosed and used TSMC's trade secret information without TSMC's consent for other purposes that were not for the mutual benefit of TSMC and Tela.

E. Tela's breach of the Powertrim Cooperation and License Agreement

32. On February 19, 2009, Tela acquired substantially all of the assets of Blaze, DFM, Inc. ("Blaze"), which had previously entered into an agreement with TSMC to develop and promote certain power reduction/optimization tools for IC design. Through this acquisition, Tela became the successor of and to all rights and duties of Blaze with respect to all agreements between Blaze and TSMC.

33. On May 18, 2010, Tela and TSMC entered into a Powertrim Cooperation and License Agreement which terminated the Joint Marketing Agreement effective as of that day. The Powertrim Cooperation and License Agreement provided that, during the term of the Agreement, and with the exception of two other Tela customers, TSMC would have an exclusive right and license even as to Tela to practice certain of Tela's Patents as needed to support the creation of integrated circuit designs that utilize gate length increases or decreases ("gate length biasing") for the manufacture of wafers, including to create and offer for use or sale cell libraries used to design gate-length-biased IC layouts. The Agreement commenced on May 18, 2010 and terminated on May 17, 2013.

34. On information and belief, in breach of the Agreement, Tela practiced the Tela Patents during the term of the Agreement to create its own cell libraries that it has offered, and continues to offer, for sale or license.

FIRST CAUSE OF ACTION

(Fraud – Deceit)

35. TSMC incorporates the allegations of paragraphs 1 through 34 as if fully set forth herein.

36. On or about March 9, 2009, Tela induced TSMC to disclose its 28 nm Design Rules to Tela by falsely representing that it would keep TSMC's Design Rule information confidential and would use it only for the mutual benefit of TSMC and Tela, when in fact, Tela intended to disclose TSMC's confidential information to its patent agents and use it to shape or

amend Tela's patent claims. Tela knew that its representation was false, and intended for TSMC to rely on it.

37. Tela intentionally failed to disclose to TSMC the material fact that it would disclose TSMC's confidential 28 nm information to its patent agents and use it to shape or amend Tela's patent claims. TSMC did not know of this fact, and Tela intended to deceive TSMC by failing to disclose it.

38. TSMC reasonably relied on Tela's false representation and material omission to provide Tela its 28 nm Design Rules and other technical information relating to its 28 nm processes on March 12, 2009.

39. Tela used TSMC's 28 nm information after March 12, 2009, to amend its continuation patent applications to claim subject matter that it did not invent, but that was designed to cover products designed in accordance with TSMC's 28 nm Design Rules. TSMC did not discover Tela's fraud until sometime in 2013.

40. TSMC has been damaged by Tela's fraud in an amount to be determined, but in excess of this Court's jurisdictional amount.

41. TSMC is entitled to damages for the actual loss caused to TSMC by Tela's fraud and/or for any unjust enrichment that Tela has enjoyed by its breach that has not been taken into account in computing damages for TSMC's actual loss.

42. TSMC has no adequate remedy at law for the present and threatened future injuries being caused by Tela's fraudulent representation and omission. TSMC, therefore, is entitled to injunctive relief to prevent Tela from making further use or disclosure of the confidential information it wrongfully obtained and the patents it secured as a result of its fraud.

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SECOND CAUSE OF ACTION
(Breach of Contract – Nondisclosure Agreements)

43. TSMC incorporates the allegations of paragraphs 1 through 42 as if fully set forth herein.

44. As stated above, Tela and TSMC entered into a Nondisclosure Agreement on May 16, 2006 and an Amended Nondisclosure Agreement on March, 9, 2009 (the "NDAs") under which they agreed to explore whether Tela's gridded array layout concept could work in conjunction with TSMC's manufacturing processes. As part of that agreement, Tela agreed only to use TSMC's confidential information for the mutual benefit of TSMC and Tela.

45. TSMC performed its obligations under the NDAs by providing confidential TSMC information to Tela and working with Tela to explore its gridded array design approach for products to be designed in accordance with TSMC's 65, 45 and 28 nm Design Rules and process technology.

46. Tela breached the NDAs by using confidential information it obtained from TSMC for purposes other than for the mutual benefit of TSMC and Tela.

47. Tela's breach has damaged TSMC in an amount to be determined, but in excess of this Court's jurisdictional amount. TSMC is entitled to damages for the actual loss caused to TSMC by Tela's breach of the NDAs, and/or for any unjust enrichment Tela has enjoyed by its breach that has not been taken into account in computing damages for TSMC's actual loss.

48. TSMC has no adequate remedy at law for the present and threatened future injuries being caused by Tela as a result of its breach of the NDAs. Tela's breach of the NDAs and wrongful acquisition of TSMC's intellectual property, as described herein, has allowed Tela unlawfully to build a reputation that it does not deserve, to enjoy intellectual property rights it has not earned, to interfere with TSMC's relationships with its customers, and to cause TSMC to incur other expenses. TSMC's injuries cannot adequately be compensated by money, and Tela lacks the resources to compensate TSMC for such continuing injuries as could be compensated by money. TSMC, therefore, is entitled to injunctive relief to prevent Tela from (1) making further use and/or disclosure of TSMC's confidential information and (2) making further use of intellectual property derived therefrom.

THIRD CAUSE OF ACTION

(Trade Secret Misappropriation - Cal. Civil Code §§ 3426 *et seq*.)

49. TSMC incorporates the allegations of paragraphs 1 through 48 as if fully set forth herein.

50. Tela has disclosed TSMC trade secret information to its attorneys and has misused TSMC trade secret information relating to TSMC's 28 nm processes – information that Tela promised in writing it would keep confidential in perpetuity.

51. TSMC's trade secrets derive independent economic value, actual or potential, from not being generally known to the public, or to other entities and persons such as Tela, who can obtain value from their disclosure or use. TSMC's knowledge and use of these trade secrets provides TSMC with competitive advantages over those who do not know them. TSMC's trade secrets are not matters either of general knowledge in the field of semiconductor processing and manufacture, nor of special knowledge to persons who are skilled in the field.

52. TSMC has made, and continues to make, efforts that are reasonable under the circumstances to protect the secrecy of its trade secrets by, among other things, requiring all recipients of TSMC's trade secret information, including Tela, to execute written nondisclosure agreements, by designating certain documents containing trade secret information as "confidential" or "restricted," and by restricting access to trade secret information to employees who need to know them, and to customers, or joint venturers, or licensees only upon their agreement to keep such information confidential.

53. Tela's misappropriation has damaged TSMC in an amount to be determined, but in excess of this Court's jurisdictional amount. TSMC is entitled to damages for the actual loss caused to TSMC by Tela's misappropriation of TSMC's trade secrets, and/or for any unjust enrichment Tela has enjoyed by such misappropriation that has not been taken into account in computing damages for TSMC's actual loss.

54. TSMC has no adequate remedy at law for the present and threatened future injuries being caused by Tela. Tela's continuing misappropriation of TSMC's trade secrets as described herein allows Tela unlawfully to build a reputation that it does not deserve, to enjoy property

rights it has not earned, and to threaten TSMC's businesses, including TSMC's relationships with its customers. Such injuries cannot adequately be compensated by money, and Tela lacks the resources to compensate TSMC for such continuing injuries as could be compensated by money. TSMC, therefore, is entitled to injunctive relief to prevent Tela from making further use and/or disclosure of TSMC's trade secrets and information derived therefrom.

55. Tela's misappropriation of TSMC's trade secrets was willful and malicious. California Civil Code Sections 3426.3(c) and 3426.4 thus entitles TSMC to an award of exemplary damages equal to twice the actual damages caused by Tela's misappropriation, as well as TSMC's reasonable attorney's fees.

FOURTH CAUSE OF ACTION

(Breach of Contract – Powertrim Cooperation and Licensing Agreement)

56. TSMC incorporates the allegations of paragraphs 1 through 55 as if fully set forth herein.

57. TSMC and Tela entered into a Powertrim Cooperation and Licensing Agreement on May 18, 2010, giving TSMC the exclusive right and license, even as to Tela, to practice certain of Tela's Patents as needed to support the creation of integrated circuit designs that utilize gate length biasing for the manufacture of wafers, including cell libraries used to facilitate and create gate-length-biased designs.

58. On information and belief, when TSMC had the exclusive right and license to practice the Tela patents during the term of the Agreement, Tela practiced the Tela Patents to create cell libraries.

59. On information and belief, Tela has offered, and continues to offer, for sale or license the cell libraries that it developed during the period of TSMC's exclusivity, in breach of the Parties' Agreement.

60. Tela's breach of the Powertrim Cooperation and Licensing Agreement has damaged TSMC in an amount to be determined, but in excess of this Court's jurisdictional amount.

61. TSMC is entitled to damages for the actual loss caused to TSMC by Tela's breach of the Powertrim Cooperation and Licensing Agreement, and/or for any unjust enrichment Tela has enjoyed by its breach that has not been taken into account in computing damages for TSMC's actual loss.

62. TSMC has no adequate remedy at law for the present and threatened future injuries being caused by Tela's breach of the Powertrim Cooperation and Licensing Agreement. Tela's breach of the agreement has enabled Tela and others to unfairly compete with TSMC. Such an injury cannot adequately be compensated by money, and Tela lacks the resources to compensate TSMC for such continuing injuries as could be compensated by money. TSMC, therefore, is entitled to injunctive relief to prevent Tela from making further use of the cell libraries that Tela developed during the term of the Powertrim Cooperation and Licensing Agreement.

PRAYER FOR RELIEF

TSMC prays for the following relief:

63. A judgment that Tela is liable on all causes of action alleged herein;

64. Damages, including disgorgement of Tela's unjust enrichment, for its breaches of contract, fraud, and trade secret misappropriation, in an amount according to proof;

65. Exemplary and punitive damages;

66. Attorneys' fees, costs, and expenses incurred by TSMC;

67. Pre-judgment and post-judgment interest;

68. Imposition of a constructive trust on any patents applied for by Tela or issued to Tela that make use of, or result from the use of, confidential information obtained from TSMC.

69. Preliminary and permanent injunctive relief enjoining Tela, its employees, or representatives, and all persons acting in concert or participating with it, as follows:

A. From disclosing any confidential information or trade secret information obtained from TSMC to any third party;

B. From using and/or gaining improper benefit from Tela's prior use of any confidential information or trade secret information obtained from TSMC for any

purpose, including to draft, amend, or enforce patent claims that Tela obtained by disclosing or misusing TSMC's confidential or trade secret information;

C. From offering to sell (or license) or selling (or licensing) to anyone, anywhere, any Tela products developed using TSMC's confidential information, or information derived therefrom; and

D. Immediately to preserve and return to TSMC (i) all copies of all TSMC documents and information, including without limitation any trade secret and other confidential or proprietary information acquired from TSMC; and (ii) all copies of all materials (in paper, electronic, or any other form) containing any, or derived from any, TSMC trade secrets or other confidential or proprietary information;

70. All other relief that the Court deems just and proper.

JURY TRIAL DEMANDED

Plaintiff demands a trial by jury of all issues so triable.

Dated: January 24, 2014

RESPECTFULLY SUBMITTED,

KEKER & VAN NEST LLP

By: /s/ *Jeffrey R. Chanin*
JEFFREY R. CHANIN
Attorney for Plaintiff Taiwan Semiconductor Manufacturing Company, Ltd.